## AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application.

**Listing of Claims:**

1. (Currently Amended) A shift register, comprising a plurality of stages connected in cascade for shifting input signals in accordance with a plurality of phase-delayed control signals, a first supply voltage, and a second supply voltage, and for applying the shifted input signals as output signals and as input signals of the succeeding ones of stages, wherein each of plurality of stages comprises:

a first controller for selectively applying an input signal and a first supply voltage to a first node arranged between first to third transistors that form a conductive path between a supply line of the input signal and an input line of the first supply voltage;

a second controller for selectively applying the first supply voltage and the second supply voltage to a second node arranged between fourth and fifth transistors forming a conductive path between an input line of the second supply voltage and the input line of the first supply voltage; and

an output buffer for selectively applying a predetermined control signal and the first supply voltage as an output signal to a stage output line sixth and seventh transistors forming a conductive path between the input line of the first supply voltage and an input line of the predetermined control signal,

wherein~~, when the fourth transistor is turned off and when the fifth transistor is turned on, the fifth transistor sustains a voltage present at the second node equal to the first supply voltage if the fourth transistor is turned off~~ the fifth transistor is controlled by a voltage of a third node arranged between the first and second transistors.

2. (Original) The shift register according to claim 1, wherein

the first and second transistors include:

first and second conductive paths, respectively, arranged between the supply line of the input signal and the first node; and

first and second control electrodes, respectively, controlling respective ones of the first and second conductive paths in accordance with the input signal and a first control signal; and

the third transistor includes:

a third conductive path arranged between the first node and the input line of the first supply voltage; and

a third control electrode controlling the third conductive path in accordance with a voltage present at the second node.

3. (Currently Amended) The shift register according to claim 2, wherein

the fourth transistor includes:

a fourth conductive path arranged between the input line of the second supply voltage and the second node; and

a fourth control electrode controlling the fourth conductive path in accordance with a second control signal; and

the fifth transistor includes:

a fifth conductive path arranged between the second node and the input line of the first supply voltage; and

a fifth control electrode controlling the conductive path in accordance with [[a]] the voltage of [[a]] the third node arranged between the first and second transistors.

4. (Original) The shift register according to claim 3, wherein each stage further comprises an eighth transistor, wherein the eighth transistor turns the fifth transistor off when the fourth transistor is turned on.

5. (Original) The shift register according to claim 4, wherein the eighth transistor includes:

an eighth conductive path arranged between the fifth control electrode of the fifth transistor and the input line of the first supply voltage; and

an eighth control electrode controlling the eighth conductive path in accordance with the second control signal.

6. (Original) The shift register according to claim 3, wherein

the sixth transistor includes a sixth conductive path arranged between an input line of a third control signal and a stage output line; and

a sixth control electrode controlling the sixth conductive path in accordance with a voltage present at the first node; and

the seventh transistor includes:

a seventh conductive path arranged between the stage output line and the input line of the first supply voltage; and

a seventh control electrode controlling the seventh conductive path in accordance with a voltage present at the second node.

7. (Original) The shift register according to claim 6, further comprising a capacitor connected between the sixth control electrode and the stage output line.

8. (Original) The shift register according to claim 2, wherein the third transistor includes a dual gate transistor having control electrodes commonly connected to the second node.

9. (Original) The shift register according to claim 3, wherein the fifth transistor includes a dual gate transistor having control electrodes commonly connected to the third node.

10. (Original) The shift register according to claim 1, wherein transistors within each stage have the same channel type.

11. (Original) The shift register according to claim 1, wherein transistors within each stage include PMOS transistors.

12. (Original) The shift register according to claim 1, wherein transistors within each stage include NMOS transistors.

13. (Original) The shift register according to claim 1, wherein the second supply voltage is higher than the first supply voltage.

14. (Original) The shift register according to claim 13, wherein the first supply voltage is about 17V.

15. (Original) The shift register according to claim 13, wherein the second supply voltage is about -8V.

16. (Original) The shift register according to claim 6, wherein the first to third control signals comprise predetermined ones of three of four clock signals, wherein first to fourth ones of the four clock signals have sequentially delayed phases, wherein a predetermined voltage is associated with each phase.

17. (Original) The shift register according to claim 16, wherein a phase of the third control signal is delayed with respect to a phase of the first control signal by one clock.

18. (Original) The shift register according to claim 16, wherein a phase of the second control signal is delayed with respect to a phase of the third control signal by two clocks.

19. (Original) The shift register according to claim 16, a phase of a portion of the input signal is equal to a phase of the first control signal.

20. (Original) The shift register according to claim 1, wherein the shift register connected to a scan driver for driving scan lines of a display device.

21. (Original) The shift register according to claim 1, wherein the shift register connected to a data driver for driving data lines of the display device.